We Claim:

1. A method for fabricating an integrated semiconductor memory having memory cells with vertical transistors, which comprises the steps of:

providing a semiconductor substrate;

depositing a first insulation layer on the semiconductor substrate;

patterning the semiconductor substrate for producing a configuration of elongate webs extending principally in a first direction and formed from a material of the semiconductor substrate and of the first insulation layer, the elongate webs being laterally isolated from one another by trenches formed in the semiconductor substrate during the patterning;

conformally depositing a gate oxide layer;

producing gate electrodes running around the elongate webs and disposed at a level of a lower region of sidewalls of the webs on the gate oxide layer;

filling the trenches with a first insulating material;

forming bit lines above the elongate webs, the bit lines crossing the elongate webs perpendicularly to the first direction and conductively connected to top sides of the elongate webs;

covering at least top sides of the bit lines with a second insulation layer;

depositing a second insulating material;

etching further trenches for forming word lines, the further trenches running parallel to the first direction, the gate electrodes being uncovered at least in an upper region due to the etching;

using an isotropic, conformal deposition process for forming a third insulation layer having a thickness less than a layer thickness of the gate electrodes on the gate oxide layer;

anisotropic etching the third insulation layer perpendicularly to a surface of the semiconductor substrate, thereby uncovering top sides of the gate electrodes; and

producing word lines running above the bit lines over the elongate webs parallel to the first direction and making contact with uncovered top sides of the gate electrodes.

2. The method according to claim 1, which further comprises covering the gate oxide layer with the third insulation layer on the sidewalls of the elongate webs above the gate electrodes.

3. The method according to claim 2, which further comprises:

forming the first insulation layer, the second insulation layer and the third insulation layer from a same material; and

setting layer thicknesses of the first insulation layer and of the second insulation layer to be thick enough such that top sides of the semiconductor substrate defining the elongate webs and the bit lines remain covered during the anisotropic etching step.

4. The method according to claim 3, which further comprises forming the first insulation layer, the second insulation layer and the third insulation layer from a material selected from the group consisting of nitrides and silicon nitride.

5. The method according to claim 1, which further comprises:

setting a height of the bit lines to be greater than a layer thickness of the first insulation layer; and

depositing the third insulation layer on uncovered sidewalls of the bit lines.

6. The method according to claim 1, which further comprises forming the gate electrodes to run around the elongate webs from an electrically conductive layer being deposited conformally and etched back anisotropically perpendicularly to the surface of the semiconductor substrate, the gate oxide layer thereby being uncovered in an upper region of the elongate webs.

7. The method according to claim 1, which further comprises producing the bit lines using a procedure in which, in accordance with a damascene technique, additional trenches are etched into the first insulation layer and into the first insulating material and are filled with a conductive material.

8. The method according to claim 1, which further comprises producing the bit lines by etching through the first insulation layer to the semiconductor substrate.

9. The method according to claim 1, which further comprises forming storage capacitors between which the elongate webs are disposed laterally.

10. The method according to claim 1, which further comprises implanting source/drain electrodes into the sidewalls of the elongate webs above the gate electrodes.

11. An integrated semiconductor memory having memory cells with vertical transistors, comprising:

a semiconductor substrate having trenches formed therein defining webs having sidewalls and a top-side formed between said trenches, said trenches isolating said webs from each other;

a first insulation layer disposed on said top-side of said webs;

an insulating material filling said trenches;

a gate oxide layer covering said sidewalls of said webs;

gate electrodes running around said webs, disposed on said gate oxide layer and having top sides, said top sides of said gate electrodes disposed to be deeper than an interface between a material of said semiconductor substrate and said first insulation layer;

a second insulation layer disposed on said gate electrodes and said webs; and

word lines formed above said webs, said word lines making contact with said top sides of said gate electrodes and isolated from said sidewalls of said webs and sidewalls of said gate electrodes by said second insulation layer.